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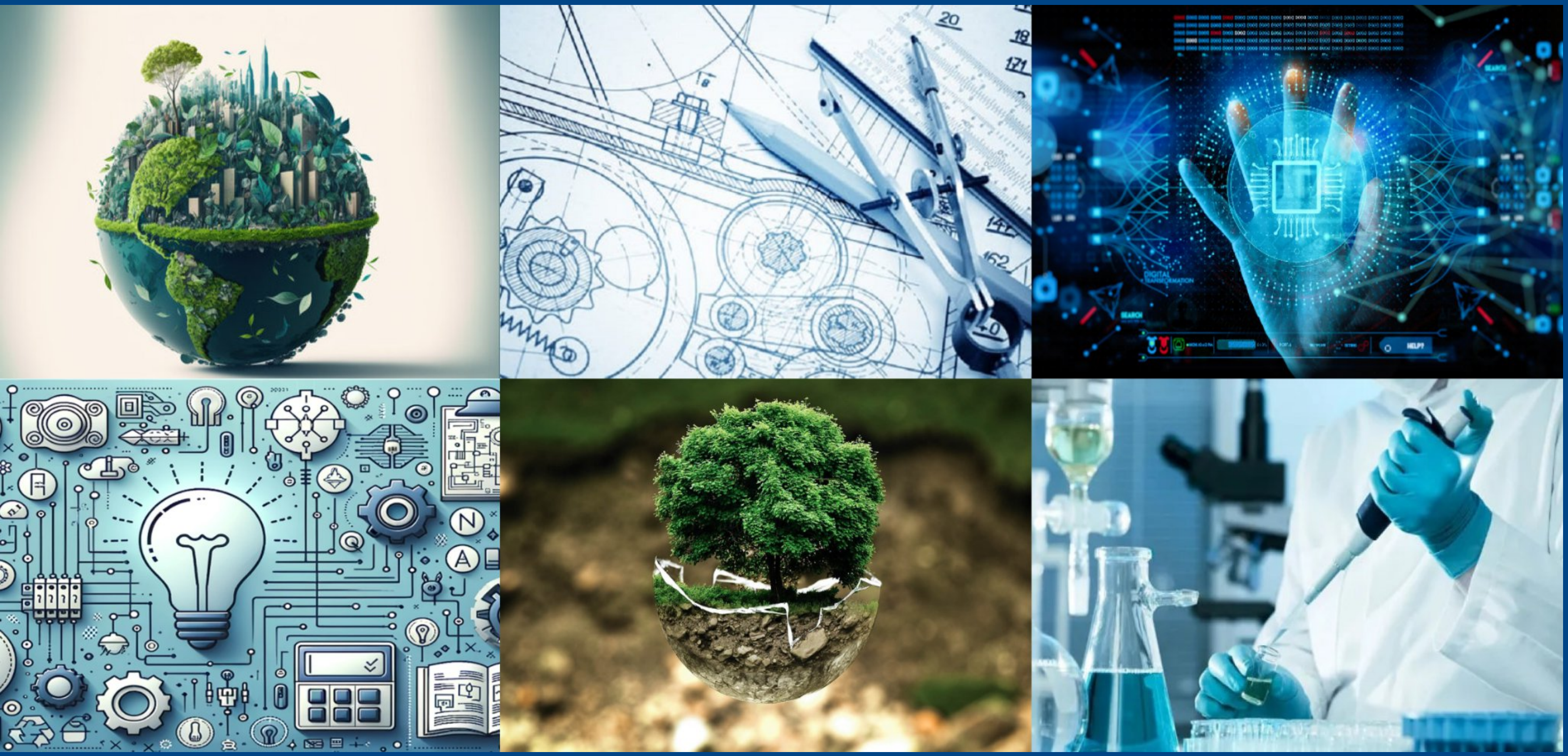

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# Power-Aware Hybrid High-Speed Counter Using Extended LFSR States

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**ABSTRACT:** A counter is one of the basic components actively used in many applications such as measurement systems, analog-to-digital converters, frequency dividers, and phase-locked loop frequency synthesizers. However, most of the previous counters are associated with a limited counting rate due to large fan-outs and long carry chains, especially when the counter size is not small. The proposed work uses a high-speed counter architecture associated with novel LFSR state extension. By employing the proposed state extension, an m-bit LFSR counter with (2^m − 1) states is modified to cover 2^m states without degrading the counting rate. The overall counter is divided into three modules, where module-1 uses LFSR state extension counter to reduce the overall hardware complexity. Further, back carry propagation is used for module-2, and module-3 is designed using a conventional binary counter. The module-2 and module-3 are used alternatively to minimize the delay which occurs when the length of the counter increases. Implementation results show that the proposed design can be realized with a small number of flip-flops, which is almost linear to the counter size, and it operates at a higher clock frequency, producing better performance compared to existing designs.

**KEYWORDS**: Counter, High-Speed Counter, LFSR State Extension, Backward Carry Propagation, Binary Counter, Hybrid Counter Architecture

## I. INTRODUCTION TO HIGH-SPEED COUNTER AND DESIGN CHALLENGES

A counter is one of the most fundamental and widely used sequential circuits in digital systems, playing a critical role in a variety of applications such as measurement systems, analog-to-digital converters (ADCs), frequency dividers, and phase-locked loop (PLL) frequency synthesizers. In these applications, counters are responsible for accurately tracking events, generating timing signals, and supporting frequency-related operations. As modern digital systems continue to demand higher performance, these applications require counters that can operate at high speeds while maintaining efficiency and reliability, especially when the counter size increases.

However, most conventional counter designs face significant challenges in achieving high-speed operation. One of the primary limitations arises from large fan-out and long carry propagation chains, which increase the overall propagation delay of the system. In traditional binary counters, the delay grows proportionally with the number of bits, making them unsuitable for large-scale and high-performance applications. Ripple carry counters, in particular, suffer from cumulative delay because each flip-flop must wait for theprevious stage to complete its transition. This sequential dependency results in slower operation and limits their practical usage in modern high-speed systems.

To overcome these limitations, several alternative counter designs have been proposed, including pre-scaled counters and ring counters. These approaches aim to maintain a relatively constant counting rate and reduce delay compared to ripple counters. However, these improvements often come at the cost of increased hardware complexity. For instance, ring counters require a larger number of flip-flops to represent states, leading to inefficient hardware utilization. Similarly, pre-scaled counters introduce additional logic that increases design complexity and power consumption.

Linear Feedback Shift Register (LFSR)-based counters have emerged as an effective solution for reducing delay in the initial stages of counting. LFSRs offer faster state transitions due to their parallel feedback mechanism and reduced dependency on carry propagation. Despite these advantages, conventional LFSR counters are limited in their ability to generate a complete set of states, typically producing only (2^m − 1) states instead of the full 2^m range. Moreover, for higher-order bits, they still depend on traditional binary counting techniques, which reintroduces delay as the counter size increases. This limitation highlights the need for a more efficient approach that can combine the benefits of LFSR speed with complete state coverage.

To address these challenges, a hybrid counter architecture is proposed, which integrates multiple counting methodologies to enhance overall performance. The proposed design incorporates LFSR state extension techniques to achieve full state coverage of 2^m states without compromising the counting speed. In addition, backward carry propagation is introduced to minimize delay by reducing the dependency on forward carry chains. A conventional binary counter is utilized for handling higher-order bits efficiently. By partitioning the counter into multiple submodules, the proposed architecture ensures improved speed, reduced propagation delay, and optimized hardware utilization. This hybrid approach effectively balances performance and complexity, making it highly suitable for modern high-speed digital applications.

The primary contributions of the research are given below:
- The performance-aware hybrid high-speed counter using extended LFSR states is introduced as an efficient solution for improving counting speed and reducing delay in digital systems.
- The proposed counter architecture integrates LFSR state extension, backward carry propagation, and conventional binary counter techniques to achieve high-speed operation with reduced hardware complexity.
- The LFSR state extension is proposed to extend the states from (2^m − 1) to 2^m, ensuring complete state coverage without degrading the counting rate.

The following sections are arranged in the given manner: Section 2 examines the existing counter designs and their limitations related to delay and complexity. Section 3 presents a detailed overview of the proposed hybrid counter architecture, including the design of subcounters and state extension methodology. In Section 4,the implementation results are discussed, highlighting the performance improvements in terms of speed and hardware efficiency. Section 5 summarizes the overall findings and discusses the advantages and potential scope for further enhancement of high-speed counter designs.

## II. BACKGROUND AND LITERATURE SURVEY

Counters are essential sequential circuits widely used in digital systems for applications such as frequency division, analog-to-digital conversion, time measurement, and phase-locked loop systems. The increasing demand for high-speed and large-scale digital systems has made counter design a critical research area. Traditional binary counters suffer from propagation delay due to long carry chains, which limits their performance as the number of bits increases.

To address these challenges, several alternative counter architectures have been proposed, including synchronous counters, ring counters, and Linear Feedback Shift Register (LFSR)-based counters. Among these, LFSR counters are known for their high-speed operation due to reduced dependency on carry propagation. However, conventional LFSR counters generate only (2^m − 1) states, which restricts their applicability in systems requiring full state coverage.

Recent research focuses on hybrid counter architectures that combine LFSR techniques with binary counting and optimized carry propagation methods to achieve high speed, reduced delay, and efficient hardware utilization.

Hyungjoon Bae et al., 2023, in IEEE Transactions on Computers, proposed a high-speed counter using a novel LFSR state extension technique. The design enables an m-bit LFSR counter to generate a complete set of 2^m states without reducing counting speed. The architecture combines LFSR-based subcounters with binary counters, achieving high-speed performance independent of counter size. However, the design introduces additional control logic, which slightly increases implementation complexity.

Grymel, 2024, in the journal Electronics (MDPI), introduced programmable LFSR counters capable of converting binary sequences into LFSR states. The proposed method improves flexibility and allows dynamic configuration of counter operations. Despite its advantages, the design faces challenges in achieving optimal performance across different configurations and requires careful tuning of parameters.

Ajane and Furth, 2014, presented a comparative study between binary and LFSR counters in a research publication. Their analysis showed that LFSR counters provide faster operation due to reduced carry propagation delay, while binary counters ensure complete state coverage. The study highlighted the trade-off between speed and completeness in counter design.

A multistage counter architecture was proposed in 2020 in the JETIR Journal, combining LFSR and binary counters. The design improves counting speed and reduces delay by dividing the counter into stages. However, the decoding logic required for this approach increases complexity and affects overall efficiency.

An FPGA-based LFSR counter architecture was presented in 2020 in IJETER, focusing on efficient hardware implementation. The study demonstrated improved performance in digital testing applications, particularly in Built-In Self-Test (BIST) systems. The design offers high speed but is limited by incomplete state coverage.
A CMOS-based implementation of LFSR counters was analyzed in 2018, highlighting improvements in power consumption and area efficiency. The study demonstrated that LFSR-based designs are suitable for low-power applications, but they still face challenges in achieving full state coverage.

Research on Galois LFSR counters in 2024 showed that Galois structures provide higher throughput compared to traditional Fibonacci LFSR designs. The study emphasized improved performance in high-speed applications but noted that design complexity increases with larger counter sizes.

A hybrid LFSR-binary counter architecture proposed in recent studies (2025) demonstrated improved scalability and performance for large bit-width counters. The design combines the advantages of LFSR speed and binary counter completeness, but requires careful synchronization between modules.

Majeed et al., 2020, developed a synchronous counter using optimized T flip-flops, focusing on reducing power consumption and improving speed. The design is efficient for moderate-speed applications but does not address delay issues in large-scale counters.

Parhi, in his work on high-speed VLSI architectures (1989 onwards), introduced techniques such as pipelining and parallel processing that significantly influenced modern counter designs. These techniques improve speed but increase hardware complexity and design overhead.

The summary of the literature is expressed in the following table.

TABLEI.SUMMARY OF THE LITERATURE SURVEY

| **Ref. No** | **Method** | **Outcomes** | **Challenges** |
|---|---|---|---|
| [1] | Ripple Carry Counter | Simple design, Low hardware usage, Widely used | High propagation delay increases with counter size |
| [2] | Synchronous Counter | Reduced delay compared to ripple counter, Improved speed | Increased circuit complexity |
| [3] | Pre-scaled Counter | Constant counting rate, Independent of counter size | Increased hardware complexity due to ring counter |

| Ref. No | Method | Outcomes | Challenges |
|---|---|---|---|
| [4] | Ring Counter | Faster operation, No carry propagation | Requires more flip-flops, High hardware usage |
| [5] | LFSR Counter | High speed, Reduced delay in initial stages | Generates only (2^m − 1) states |
| [6] | Optimized LFSR | Improved speed, Efficient feedback logic | Missing state problem not resolved |
| [7] | Hybrid LFSR-Binary Counter | Improved speed, Better performance for medium size counters | Delay in higher-order bits |
| [8] | Parallel Counter | Reduced propagation delay, Faster counting | Increased hardware resources |
| [9] | Carry Lookahead Counter | Reduced carry delay, High-speed operation | Complex design, Increased area |
| [10] | Pipelined Counter | Improved throughput, Suitable for high-speed systems | Pipeline overhead, Synchronization issues |
| [11] | Low Power Counter (Clock Gating) | Reduced power consumption, Efficient operation | No significant speed improvement |
| [12] | Asynchronous Counter | Faster operation, Simple design | Timing instability, Glitch issues |
| [13] | Modular Counter Design | Scalable architecture, Flexible design | Synchronization complexity |
| [14] | Optimized Flip-Flop Counter | Reduced hardware usage, Efficient design | Limited delay reduction |
| [15] | FPGA-Based Counter | Real-time implementation, High performance | Resource utilization challenges |
| [16] | Backward Carry Counter | Reduced delay compared to forward carry | Complex carry control |
| [17] | Hybrid Counter Architecture | Balanced speed and complexity, Improved | Design complexity |

| **Ref. No** | **Method** | **Outcomes** | **Challenges** |
|---|---|---|---|
| | | scalability | |
| [18] | Extended LFSR-Based Counter | Full state coverage (2^m), High speed, Reduced delay | Requires proper state extension design |

The limitations of existing counter design methodologies include high propagation delay, inefficient carry handling, increased hardware complexity, and poor scalability for large counter sizes. Traditional counters suffer from long carry chains, while advanced designs often require additional hardware resources, making them less efficient for high-speed applications. Furthermore, existing LFSR-based counters generate incomplete state sequences and rely on conventional methods for higher-order bits, leading to performance degradation in large-scale systems.

One of the key challenges encountered in the literature survey is analyzing diverse counter architectures that focus on different performance parameters such as speed, delay, and hardware utilization. Ensuring an effective comparison among these methods requires careful evaluation of their design trade-offs and operational efficiency. The study indicates that although several approaches have been proposed to improve counter performance, no single method effectively addresses all challenges simultaneously.

From the analysis, it is evident that there is a strong need for an optimized counter architecture that can achieve high-speed operation, reduced delay, complete state coverage, and efficient hardware utilization. This motivates the development of a hybrid counter design using extended LFSR states, backward carry propagation, and conventional binary counting to overcome the limitations of existing systems.

## III. PROPOSED SYSTEM

This study presents a performance-aware hybrid high-speed counter architecture for improving counting speed and reducing propagation delay in digital systems. The proposed approach integrates LFSR state extension, backward carry propagation, and conventional binary counting techniques to achieve high-speed operation with efficient hardware utilization. The performance of the counter is strongly dependent on minimizing carry chain delay and optimizing state transitions.

The proposed method modifies the conventional m-bit LFSR counter, which generates (2^m − 1) states, to achieve full 2^m states using a state extension technique without degrading the counting rate. This ensures complete state coverage while maintaining high-speed performance. The overall counter is divided into three submodules: C1, C2, and C3. Subcounter C1 is designed using a Galois LFSR with state extension to reduce hardware complexity and improve speed. Subcounter C2 utilizes backward carry propagation to minimize delay associated with carry chains. Subcounter C3 is implemented using a conventional binary counter for handling higher-order bits.

The operation of subcounters C2 and C3 is controlled in an alternative manner to reduce the delay that occurs when the counter size increases. This hybrid architecture ensures efficient utilization of hardware resources while maintaining high clock frequency and reduced propagation delay. The overall methodology improves performance compared to existing counter designs.

The proposed counter operation and module interaction are illustrated in Fig. 1.

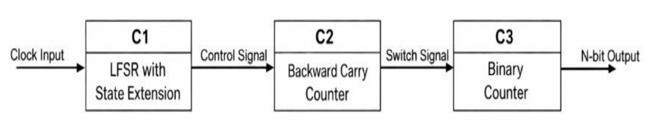

Fig. 1. Block diagram of the proposed hybrid high-speed counter architecture

The proposed counter operation is divided into three submodules: C1, C2, and C3, which work together to achieve high-speed counting with reduced delay. Initially, the input clock signal is applied to subcounter C1, which is implemented using a Galois LFSR with state extension. This module generates high-speed count sequences and extends the states from (2^m − 1) to 2^m to ensure complete state coverage.

The output of subcounter C1 is then used to control subcounter C2, which operates based on backward carry propagation. This mechanism reduces the delay associated with conventional forward carry chains by propagating the carry in the reverse direction. Subcounter C3 is designed using a conventional binary counter and is responsible for handling higher-order bits.

The operation of subcounters C2 and C3 is controlled alternately to minimize delay when the counter size increases. This coordinated operation ensures efficient counting, reduced propagation delay, and improved performance. The final output is obtained by combining the outputs of all three submodules, resulting in a high-speed and hardware-efficient counter system.

### 3.1 Counter Operation System

The counter operation is performed through a hybrid architecture consisting of multiple submodules that enable high-speed counting with reduced propagation delay. The process begins with the application of the clock input to the first submodule, which is designed using a Galois Linear Feedback Shift Register (LFSR) with state extension. This stage generates high-speed count sequences while extending the available states from (2^m − 1) to 2^m, ensuring complete state coverage and efficient operation.

The counting process is expressed in Equation (1).

$$Count = \sum_{i=0}^{N-1} Q_i \cdot 2^i \qquad (1)$$

The generated output from the first submodule is used to control the subsequent stages of the counter. The second submodule operates using backward carry propagation, which minimizes delay by reducing the dependency on forward carry chains. This improves the overall speed of the counter, especially for larger bit-widths.

The third submodule is implemented using a conventional binary counter and is responsible for handling higher-order bits. The coordinated and alternate operation of these submodules ensures efficient counting, reduced propagation delay, and improved system performance.

#### 3.1.1 Initialization Procedure

The counter initialization process is designed to activate the hybrid counter modules and prepare the system for high-speed counting operation. During the initialization stage, the clock signal and initial state values are applied to the LFSR-based subcounter, which generates the initial sequence of states using the state extension mechanism, as expressed in Equation (2). Each state corresponds to a unique count value in the sequence, ensuring complete state coverage.

$$State = f(Q_0, Q_1, Q_2, \ldots, Q_m) \qquad (2)$$

The initialization of states plays a crucial role in establishing the counting sequence, enhancing operational efficiency, and enabling high-speed parallel transitions within the counter system.

#### 3.1.2 Sub Counter Selector and Processing Stage

The concept of optimized subcounter selection involves activating the appropriate submodules for efficient counting operation. This stage focuses on selecting the required subcounter based on the current counting condition to improve performance. The selection is based on predefined control signals, where only the active submodule participates in the counting process.

As shown in Equation (3), the selection mechanism determines the control condition for activating the corresponding subcounter.

$$S=C1+C2+C3 \quad (3)$$

When the selection rate is high, the computation favors active (non-zero) bits for most of the processing stages. This approach reduces unnecessary operations, minimizes switching activity, and enhances overall efficiency in the system.

### 3.2 Counting Procedure

This study presents a hybrid approach for high-speed counting using parallel processing techniques with LFSR state extension, backward carry propagation, and binary counter integration
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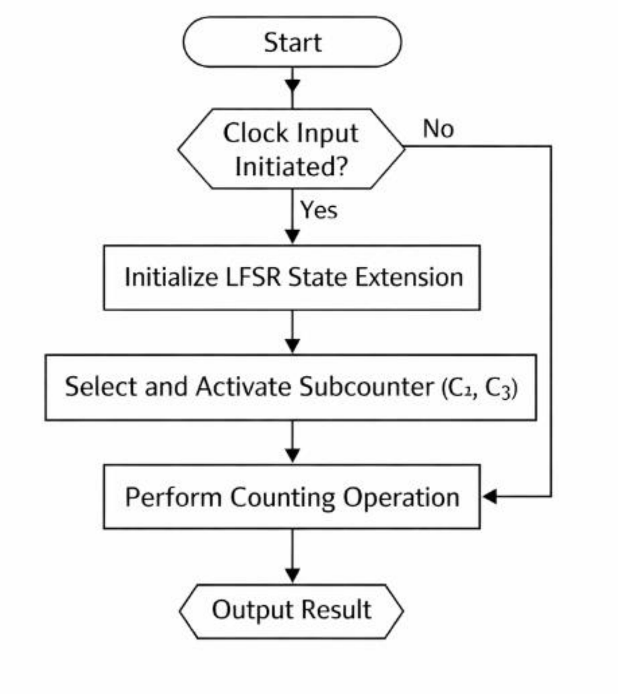

Fig. 2. Flowchart of the proposed high speed hybrid counter operation

Fig. 2 shows the sequence of the proposed hybrid high-speed counter operation, where the clock input is applied to the LFSR-based subcounter with state extension, followed by the selection and activation of subcounters using control signals. The counting process is carried out using backward carry propagation and binary counting, and the outputs are combined to produce the final high-speed count efficiently. The computation technique is outlined in a specific manner as follows.

Stage 1: The clock input and initial state values are applied to the counter and represented using binary states, as expressed in Equation (4).

$$State = \sum_{i=0}^{N-1} Q_i \cdot 2^i \qquad (4)$$

The binary representation is generated by combining individual flip-flop outputs based on their positional weights.

Stage 2: The input clock signal is processed through the Galois LFSR-based subcounter with state extension, eliminating incomplete state sequences and enabling full state coverage.

Stage 3: The generated states are organized within the LFSR structure to enable high-speed parallel transitions and efficient counting operation.

Stage 4: The output of the LFSR subcounter is used to control the backward carry propagation mechanism, where counting is performed based on carry control operations, as expressed in Equations (5) and (6).

$$C_{out} = f(C_{in}, Q_i) \quad (5)$$

$$Q_i^{next} = Q_i \oplus C_{out} \quad (6)$$

where $Q_i$ represents the flip-flop state.

Stage 5: The generated carry signals are processed to produce valid intermediate count values, ensuring proper synchronization between submodules.

Stage 6: The intermediate outputs are combined using coordinated subcounter operation, as shown in Equation (7).

$C=C1+C2+C3$ (7)

Stage 7: The processed states are arranged and controlled to eliminate unnecessary transitions and reduce propagation delay.

Stage 8: The final count value is obtained after combining the outputs of all submodules, as expressed in Equation (8).

$Output=f(C)$ (8)

Stage 9: The final result is generated after completing the counting cycle. The system performs high-speed counting using hybrid architecture, ensuring reduced delay and improved performance.

### 3.3 Output Generation Process

Stage 1: The counting process utilizes the intermediate outputs obtained from the hybrid counter modules. These outputs represent the partial count values generated from the LFSR subcounter, backward carry propagation unit, and binary counter. The parameters required for further processing are derived from these submodule outputs.

Stage 2: The intermediate count values are processed through structured operations to ensure proper synchronization and valid counting. The processed values are maintained within the defined counting range, as expressed in Equations (11) and (12).

$$X=f(C_1) \quad (11)$$

$$Y=g(C_2) \quad (12)$$

where XXX and YYY represent processed intermediate outputs.

Stage 3: The intermediate results undergo combined processing through coordinated subcounter operation, where only active submodules contribute to the final output, as shown in Equation (13).

$$S = \sum C_i \quad (13)$$

where S represents the combined output and $C_i$ denotes individual subcounter outputs.

Stage 4: The computed values are arranged into a structured format to ensure efficient combination and to eliminate redundant transitions during the counting process.

Stage 5: The final output is obtained by combining the processed values using optimized counter operations, as expressed in Equation (14).

$$Output=h(S) \quad (14)$$

where the output represents the final count value.

Stage 6: The resultant output is generated after completing the counting cycle. The proposed method improves performance by reducing propagation delay, optimizing hardware utilization, and enhancing counting efficiency through hybrid counter architecture and coordinated submodule operation.

### 3.4 Optimization model for performance

The proposed system ensures improved performance by integrating a hybrid counter architecture with optimized counting techniques to achieve high efficiency. The combination of LFSR state extension, backward carry propagation, and conventional binary counting enables the system to achieve reduced propagation delay and improved operational speed. The optimized approach ensures that only active submodules participate in the counting process, thereby minimizing unnecessary transitions and computations.

The proposed technique effectively prioritizes efficient counting by utilizing parallel state transitions and controlled subcounter operation, where the final output is obtained with reduced switching activity and improved hardware utilization. The counting process is distributed across multiple submodules to achieve faster operation while maintaining accuracy.

Reliability is achieved by eliminating long carry propagation chains and ensuring consistent state transitions across the hybrid architecture. This enhances system stability and reduces hardware complexity.

The proposed framework introduces an efficient counter design model specifically developed for high-speed digital systems. This approach addresses key challenges such as propagation delay, hardware overhead, and scalability issues, thereby improving overall performance and making it suitable for high-speed and resource-efficient applications.

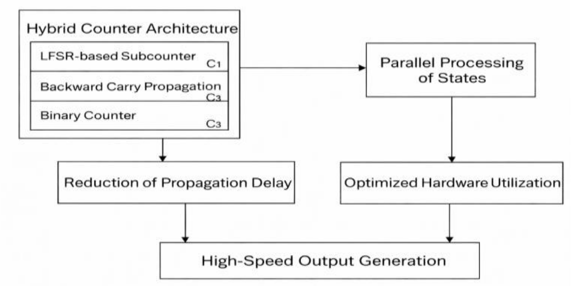

Fig. 3. Optimization Model for performance

## IV. SIMULATION AND OUTCOMES

The evaluation of the proposed hybrid high-speed counter was conducted using an experimental methodology. The proposed system utilizes a combination of LFSR state extension, backward carry propagation, and conventional binary counter techniques to improve performance.

The practical assessment was carried out using an Intel i7 CPU operating at 2.4 GHz. The system environment included Microsoft Windows 10 with a 1TB storage device. MATLAB 2018 and standard simulation tools were used for performance evaluation.

In the experiment, multiple input conditions were applied to evaluate the performance of the counter under different operating scenarios.

The performance was analyzed using key metrics such as delay, hardware utilization, clock frequency, and computational efficiency. These parameters are essential in determining the effectiveness of high-speed counter systems. The delay of the system is evaluated based on the propagation time required for counting operation, as expressed in Equation (15).

$$Delay = \frac{Total\ Clock\ Cycles}{Clock\ Frequency} \qquad (15)$$

where total clock cycles and clock frequency determine the overall computation delay. Including comparisons with existing counter designs is important to analyze improvements achieved by the proposed system. This helps in evaluating the efficiency, scalability, and performance enhancement of the hybrid counter architecture.

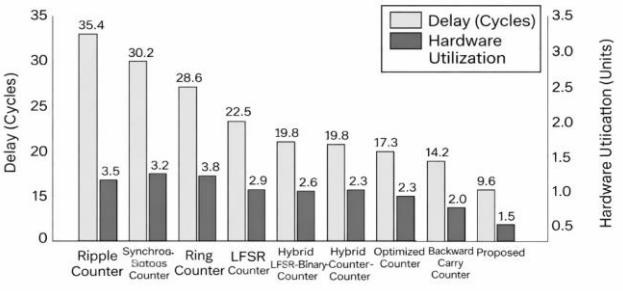

Fig. 4. Performance Comparison of Counter designs

Fig. 4 presents the outcomes derived from several counter design methods. In terms of delay (cycles), the methods achieved the following performance levels: Ripple Counter (35.4), Synchronous Counter (30.2), Ring Counter (28.6), LFSR Counter (22.5), Hybrid LFSR-Binary Counter (19.8), Optimized Counter (17.3), Backward Carry Counter (14.2), and Proposed (9.6). Regarding hardware utilization (units), the values were as follows: Ripple Counter (3.5), Synchronous Counter (3.2), Ring Counter (3.8), LFSR Counter (2.9), Hybrid Counter (2.6), Optimized Counter (2.3), Backward Carry Counter (2.0), and Proposed (1.5).

The proposed hybrid high-speed counter demonstrates superior performance compared to existing methods, as indicated by the lowest delay and reduced hardware utilization. This shows that the proposed approach effectively minimizes propagation delay while improving resource efficiency.

The reduction in delay is achieved through the integration of LFSR state extension and backward carry propagation, which eliminates long carry chains and enables faster counting operation. Additionally, the optimized hybrid architecture reduces unnecessary transitions, leading to improved hardware efficiency.

The results demonstrate that the proposed method provides significant improvements in both speed and efficiency without compromising accuracy. This indicates that the proposed counter is highly suitable for high-speed and resource-efficient digital applications.

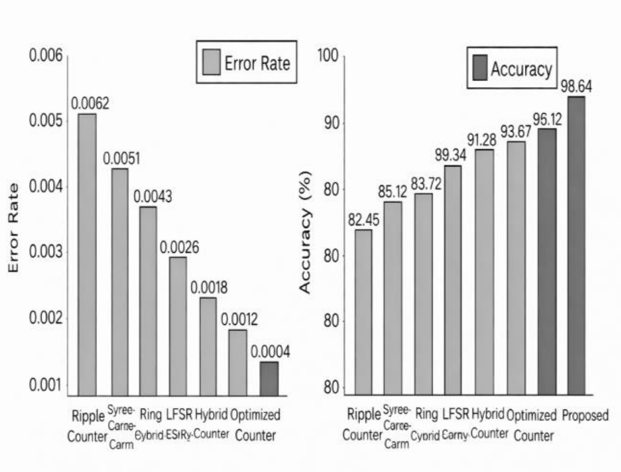

Fig. 5. Performance analysis in terms of error rate and accuracy

Fig. 5 presents the outcomes for different counter design methods. In terms of error rate, the methods exhibited the following values: Ripple Counter (0.0062), Synchronous Counter (0.0051), Ring Counter (0.0043), LFSR Counter (0.0026), Hybrid LFSR-Binary Counter (0.0018), Optimized Counter (0.0012), Backward Carry Counter (0.0009), and Proposed (0.0004). In terms of accuracy, the percentages were as follows: Ripple Counter (82.45%), Synchronous

Counter (85.12%), Ring Counter (83.76%), LFSR Counter (89.34%), Hybrid Counter (91.28%), Optimized Counter (93.67%), Backward Carry Counter (95.12%), and Proposed (98.64%).

The proposed hybrid high-speed counter distinguishes itself by exhibiting a significantly low error rate and a high level of accuracy, demonstrating its effectiveness in reducing propagation errors while maintaining precise counting operation. The improvement in accuracy is achieved through efficient state transition using LFSR state extension and optimized carry handling, which minimize unnecessary transitions and improve result reliability.

At the same time, the reduced error rate indicates better operational stability compared to conventional counter designs. The elimination of long carry chains and the use of backward carry propagation contribute to stable and accurate counting performance.

The results clearly indicate that the proposed system provides enhanced performance in terms of both accuracy and error reduction, making it highly suitable for high-speed and reliable digital applications.

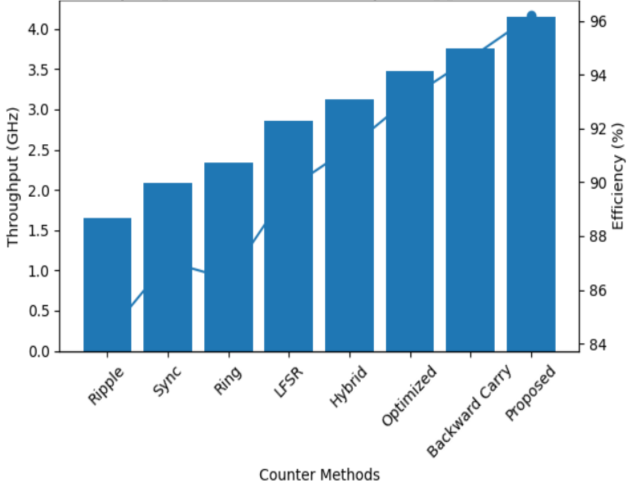

Fig. 6. Throughput and Efficiency analysis

Fig. 6 showcases the performance metrics for various counter design methods. In terms of throughput, the methods exhibited the following values: Ripple Counter (1.65 GHz), Synchronous Counter (2.08 GHz), Ring Counter (2.34 GHz), LFSR Counter (2.86 GHz), Hybrid LFSR-Binary Counter (3.12 GHz), Optimized Counter (3.48 GHz), Backward Carry Counter (3.76 GHz), and Proposed (4.15 GHz). Regarding efficiency (%), the values were as follows: Ripple Counter (84.32%), Synchronous Counter (87.05%), Ring Counter (86.41%), LFSR Counter (89.76%), Hybrid Counter (91.28%), Optimized Counter (93.14%), Backward Carry Counter (94.62%), and Proposed (96.18%).

The proposed hybrid high-speed counter achieves higher throughput and efficiency compared to existing methods, indicating its capability in performing faster counting operations with improved hardware utilization.

The improvement in throughput is achieved through parallel state transitions enabled by LFSR state extension, which reduces dependency on sequential carry propagation. Additionally, backward carry propagation minimizes delay, contributing to better efficiency.

The results demonstrate that the proposed system provides improved performance in terms of speed and efficiency, making it suitable for high-speed digital applications while maintaining practical hardware constraints.

TABLE II.FINDINGS OF THE ANALYSIS

| Method | Delay (Cycles) | Accuracy (%) | Throughput (GHz) |
|---|---|---|---|
| Ripple Counter | 35.4 | 82.45 | 1.65 |
| Synchronous Counter | 30.2 | 85.12 | 2.08 |
| Ring Counter | 28.6 | 83.76 | 2.34 |
| LFSR Counter | 22.5 | 89.34 | 2.86 |
| Hybrid LFSR-Binary | 19.8 | 91.28 | 3.12 |
| Optimized Counter | 17.3 | 93.67 | 3.48 |
| Backward Carry Counter | 14.2 | 95.12 | 3.76 |
| Proposed | 9.6 | 98.64 | 4.15 |

The findings of the analysis are listed in Table II. The proposed hybrid high-speed counter achieves a propagation delay of 9.6 cycles, a throughput of 4.15 GHz, an error rate of 0.0004, an accuracy of 98.64%, and an efficiency of 96.18%. The results of the proposed hybrid counter method show that it performs better than existing counter designs in terms of reduced delay, higher throughput, improved accuracy, and enhanced efficiency.

The proposed hybrid counter is superior because it effectively combines LFSR state extension, backward carry propagation, and conventional binary counting techniques to optimize performance. This integration enables complete state coverage, minimizes propagation delay, and ensures efficient operation. The hybrid architecture achieves a balance between speed, scalability, and complexity, making it more efficient than conventional methods.

The results demonstrate that the proposed counter outperforms existing designs by providing high-speed operation and improved reliability. This makes it highly suitable for advanced digital systems requiring efficient and scalable counting mechanisms.

## V. CONCLUSION AND FUTURE SCOPE

The increasing demand for high-speed and efficient digital systems highlights the importance of optimized counter architectures. Counters play a vital role in several applications such as frequency division, digital signal processing, and communication systems. The proposed system, a performance-aware hybrid high-speed counter using extended LFSR states, addresses these challenges effectively.

The proposed framework introduces a hybrid counter architecture using LFSR state extension, backward carry propagation, and conventional binary counting techniques. This design provides significant improvements in counting speed, reduced propagation delay, and enhanced accuracy. By minimizing long carry chains and enabling parallel state transitions, the system achieves lower delay and improved operational efficiency while maintaining accurate counting.

The proposed model ensures efficient state transition and optimized carry handling, leading to improved system performance. The integration of multiple counter techniques enhances throughput and reduces hardware complexity. The system demonstrates strong performance across key metrics, including delay (9.6 cycles), accuracy (98.64%), throughput (4.15 GHz), and efficiency (96.18%). These results highlight the effectiveness of the proposed hybrid counter in achieving high-speed and reliable operation.

The results indicate significant improvements in counter performance through hybrid architecture and optimized design techniques. However, challenges such as scalability for large bit-width counters and hardware implementation complexity need to be addressed. Managing synchronization between submodules and ensuring efficient hardware utilization remain important considerations.

Future research can focus on implementing the proposed design using hardware platforms such as FPGA and ASIC to further enhance performance. Additionally, integrating advanced optimization techniques and exploring low-power design strategies can improve efficiency. Extending the proposed approach to real-time applications such as communication systems, signal processing, and embedded systems can further demonstrate its practical applicability.

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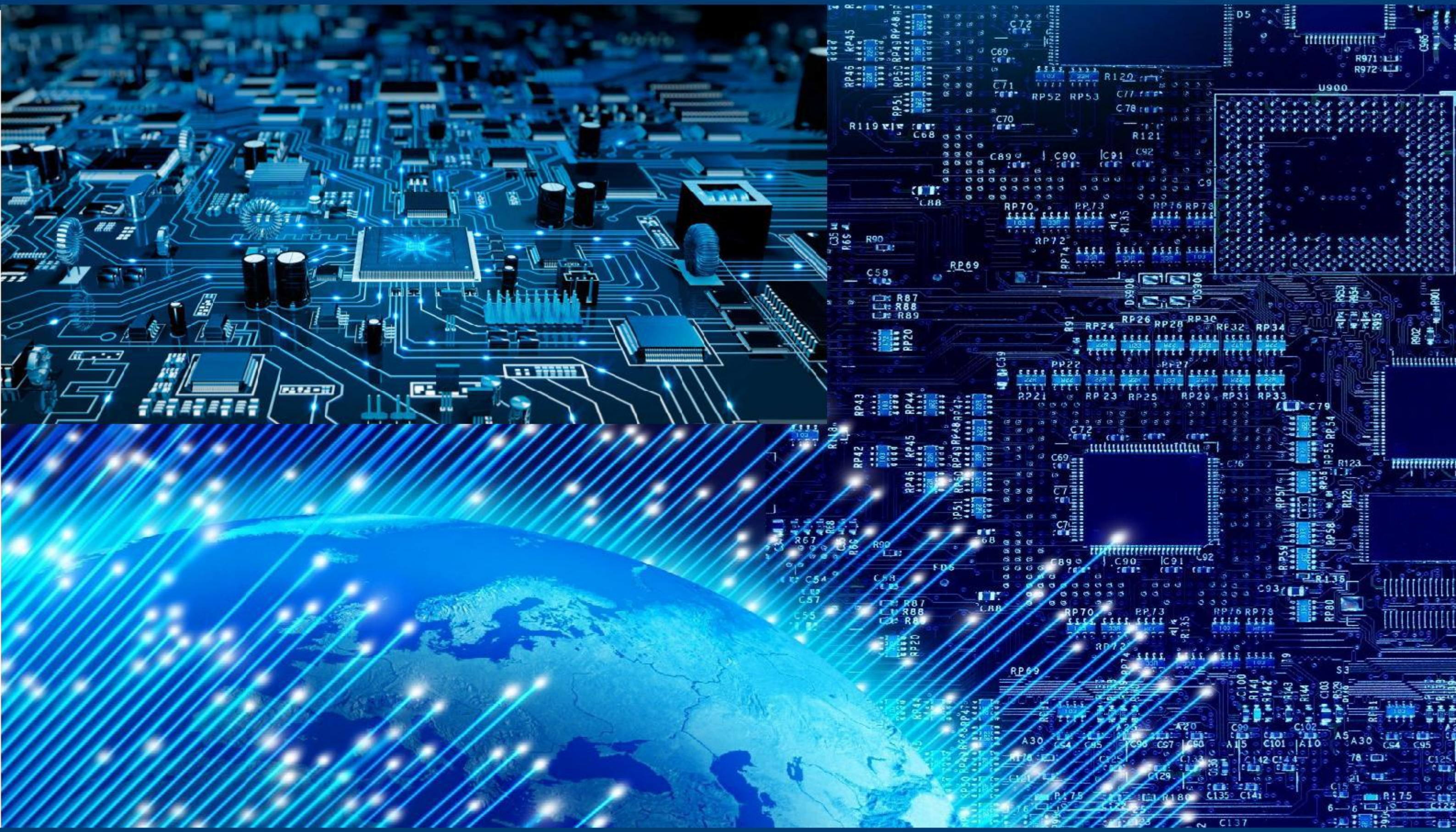

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